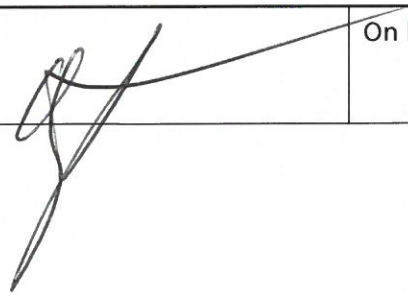
APPENDIX 4: TYPE VERIFICATION TEST REPORT

Type Approval and manufacturer declaration of compliance with the requirements of Engineering Recommendation G83/2			
SSEG Type reference number	Turbo 1P Mini, Turbo 1P		
SSEG Type	PV inverter		
Manufacturer	Steca Elektronik GmbH		
Address:	Mammostrasse 1 87700 Memmingen Germany		
Tel	+49 8331 8558-833	Fax	+49 8331 8558-132
e-mail	hotline@stecasolar.com service@stecasolar.com	Web site	www.steca.com
Maximum rated capacity	2.0 / 3.6	kW single phase	
SSEG manufacturer declaration: I certify on behalf of the company named above as a manufacturer of Small Scale Embedded Generators, that all products manufactured by the company with the above SSEG Type reference number will be manufactured and tested to ensure that they perform as stated in this Type Verification Test Report, prior to shipment to site and that no site modifications are required to ensure that the product meets all the requirements of G83/2.			
Signed		On behalf of	ppa. Ralf Griepentrog Head of R&D

Power Quality. Harmonics						
SSEG rating per phase (rpp)				kW	NV = MV * 3.68 / rpp	
Harmonic	At 45-55% of rated output		100% of rated output			
	Measured Value (MV) in Amps	Normalized Value (NV) in Amps	Measured Value (MV) in Amps	Normalized Value (NV) in Amps	Limits in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
2	0.0062	0.0125	0.0109	0.0218	1.080	
3	0.2644	0.5288	0.0437	0.0874	2.300	
4	0.0023	0.0047	0.0062	0.0125	0.430	
5	0.2215	0.4430	0.0608	0.1217	1.140	
6	0.0016	0.0031	0.0047	0.0094	0.300	
7	0.0889	0.1778	0.0078	0.0156	0.770	
8	0.0008	0.0016	0.0031	0.0062	0.230	
9	0.0889	0.1778	0.0351	0.0702	0.400	
10	0.0008	0.0016	0.0023	0.0047	0.184	
11	0.0273	0.0546	0.0086	0.0172	0.330	
12	0.0008	0.0016	0.0016	0.0031	0.153	
13	0.0374	0.0749	0.0265	0.0530	0.210	
14	0.0008	0.0016	0.0008	0.0016	0.131	
15	0.0140	0.0281	0.0094	0.0187	0.150	
16	0.0008	0.0016	0.0008	0.0016	0.115	
17	0.0218	0.0437	0.0187	0.0374	0.132	
18	0.0008	0.0016	0.0016	0.0031	0.102	
19	0.0055	0.0109	0.0133	0.0265	0.118	
20	0.0008	0.0016	0.0016	0.0031	0.092	
21	0.0047	0.0094	0.0148	0.0296	0.107	0.160
22	0.0008	0.0016	0.0016	0.0031	0.084	
23	0.0094	0.0187	0.0125	0.0250	0.098	0.147
24	0.0008	0.0016	0.0016	0.0031	0.077	
25	0.0062	0.0125	0.0109	0.0218	0.090	0.135
26	0.0008	0.0016	0.0016	0.0031	0.071	
27	0.0047	0.0094	0.0140	0.0281	0.083	0.124
28	0.0008	0.0016	0.0008	0.0016	0.066	
29	0.0062	0.0125	0.0109	0.0218	0.078	0.17
30	0.0008	0.0016	0.0008	0.0016	0.061	

31	0.0070	0.0140	0.0125	0.0250	0.073	0.109
32	0.0008	0.0016	0.0008	0.0016	0.058	
33	0.0016	0.0031	0.0109	0.0218	0.068	0.102
34	0.0008	0.0016	0.0008	0.0016	0.054	
35	0.0094	0.0187	0.0133	0.0265	0.064	0.096
36	0.0008	0.0016	0.0008	0.0016	0.051	
37	0.0156	0.0312	0.0125	0.0250	0.061	0.091
38	0.0008	0.0016	0.0008	0.0016	0.048	
39	0.0117	0.0234	0.0133	0.0265	0.058	0.087
40	0.0008	0.0016	0.0008	0.0016	0.046	

Measured by
Bureau Veritas CPS Germany GmbH
Businesspark A96
86842 Tuerkheim
Germany
with StecaGrid 1800

Power Quality. Voltage Fluctuations and Flicker								
	Starting			Stopping			Running	
	d_{max}	d_c	$d_{(t)}$	d_{max}	d_c	$d_{(t)}$	P_{st}	P_{lt} 2 hours
Measured Values	3.7	2.9	0.02	3.7	2.9	0.02	0.385	0.385
Normalised to standard impedance and 3.68kW for multiple units								
Limits set under BS EN 61000-3-2	4%	3.3%	3.3% 500ms	4%	3.3%	3.3% 500ms	1.0	0.65
Test start date	12th of Feb.2014			Test end date		12th of Feb.2014		
Test location	Bureau Veritas CPS Germany GmbH Businesspark A96 86842 Tuerkheim Germany							

Power Quality. DC injection				
Test power level	10%	55%	100%	
Recorded value	17mA	10mA	18mA	
as % of rated AC current	0.21%	0.13%	0.23%	
Limit	0.25%	0.25%	0.25%	
Measured with StecaGrid 1800				

Power Quality. Power factor				
	216.4V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within ±1.5% of the stated level during the test.
Measured value	<0.99	<0.99	<0.99	
Limit	>0.95	>0.95	>0.95	

Protection. Frequency tests						
Function	Settings		Trip test		"No trip tests"	
	Frequency	Time delay	Frequency	Time delay	Frequency / time	Confirm no trip
U/F stage 1	47.5Hz	20s	47,46 Hz	20,3 s	47.7Hz 25s	confirm
U/F stage 2	47hz	0.5s	46,94 Hz	0,8 s	47.2Hz 19.98s	confirm
					46.8Hz 0.48s	confirm
O/F stage 1	51.5Hz	90s	51,56 Hz	90,3 s	51.3Hz 95s	confirm
O/F stage 2	52Hz	0.5s	52,08 Hz	0,78 s	51.8Hz 89.98s	confirm
					52.2Hz 0.48s	confirm

Protection. Voltage tests						
Function	Settings		Trip test		"No trip tests"	
	Voltage	Time delay	Voltage	Time delay	Voltage / time	Confirm no trip
U/V stage 1	200.1V	2.5s	199,8V	2,7s	204.1V 3.5s	confirm
U/V stage 2	184V	0.5s	182,7V	0,7s	188 2.48s	confirm
					180V 0.48s	confirm
O/V stage 1	262.2V	1.0s	264,7V	1,2s	258.2V 2.0s	confirm
O/V stage 2	273.3V	0.5s	275,7V	0,7s	269.7V 0.98s	confirm
					277.7V 0.48s	confirm

Protection. Loss of Mains test						
To be carried out at three power levels with a tolerance of plus or minus 5% in Test Power levels						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Limit is 0.5 seconds	N/A	N/A	N/A	N/A	N/A	N/A
For multi phase SSEG s confirm that the device shuts down correctly after the removal of a single fuse as well as operation on all phases						
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph1 fuse removed	N/A	N/A	N/A	N/A	N/A	N/A
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph2 fuse removed	N/A	N/A	N/A	N/A	N/A	N/A
Test Power	10%	55%	100%	10%	55%	100%
Balancing load on islanded network	95% of SSEG output	95% of SSEG output	95% of SSEG output	105% of SSEG output	105% of SSEG output	105% of SSEG output
Trip time. Ph3 fuse removed	N/A	N/A	N/A	N/A	N/A	N/A
Note for technologies which have a substantial shut down time this can be added to the 0.5 seconds in establishing that the trip occurred in less than 0.5s. Maximum shut down time could therefore be up to 1.0seconds for these technologies.						
Indicate additional shut down time included in above results.						ms
Note as an alternative, inverters can be tested to BS EN 62116. The following sub sets of tests should be recorded in the following table						
Time Power and imbalance	33% -5% Q Test 22	66% -5% Q Test 12	100% -5% Q Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% Q Test 10
Trip time. Limit is 0.5 seconds	0.71s	0.96s	0.81s	0.97s	0.82s	0.86s

Protection. Frequency change, Stability test				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		confirm
Negative Vector Shift	50.5Hz	-9 degrees		confirm
Positive Frequency drift	49.5Hz	+0.19Hz/s	51.5Hz	confirm
Negative Frequency drift	50.5Hz	-0.19Hz/s	47.5Hz	confirm

Protection. Re-connection timer						
Test should prove that the reconnection sequence starts after a minimum delay 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1						
Time delay setting	Measured delay		Check on no reconnection when the voltage or frequency is brought to outside stage 1 limits of table 1			
			At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirm that the SSEG does not re-connect			confirm	confirm	confirm	confirm

Fault level contribution					
For a directly coupled SSEG			For an Inverter SSEG		
Parameter	Symbol	Value	Time after fault	Volts	Amps
Peak Short Circuit current	i_p	N/A	20ms	79,15	16,65
Initial Value of aperiodic current	A	N/A	100ms	73,03	10,54
Initial symmetrical short-circuit current	I_k	N/A	250m	72,78	9,48
Decaying (aperiodic) component of a short circuit current	i_{DC}	N/A	500m	72,77	9,40
Reactance/Resistance Ratio of source	X/R	N/A	Time to trip	0,757	In seconds
Measured by Bureau Veritas CPS Germany GmbH Businesspark A96 86842 Tuerkheim Germany					

Self-monitoring solid state switching	Yes or N/A
It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0.5 seconds.	N/A

Additional comments
Unless otherwise noted all testing were done in the laboratories of the manufacturer and with the StecaGrid 3600, which is regarded either as representative or as worst case.